Coverage Improvement of Assertion Based SDC Verification at Early Design Phase

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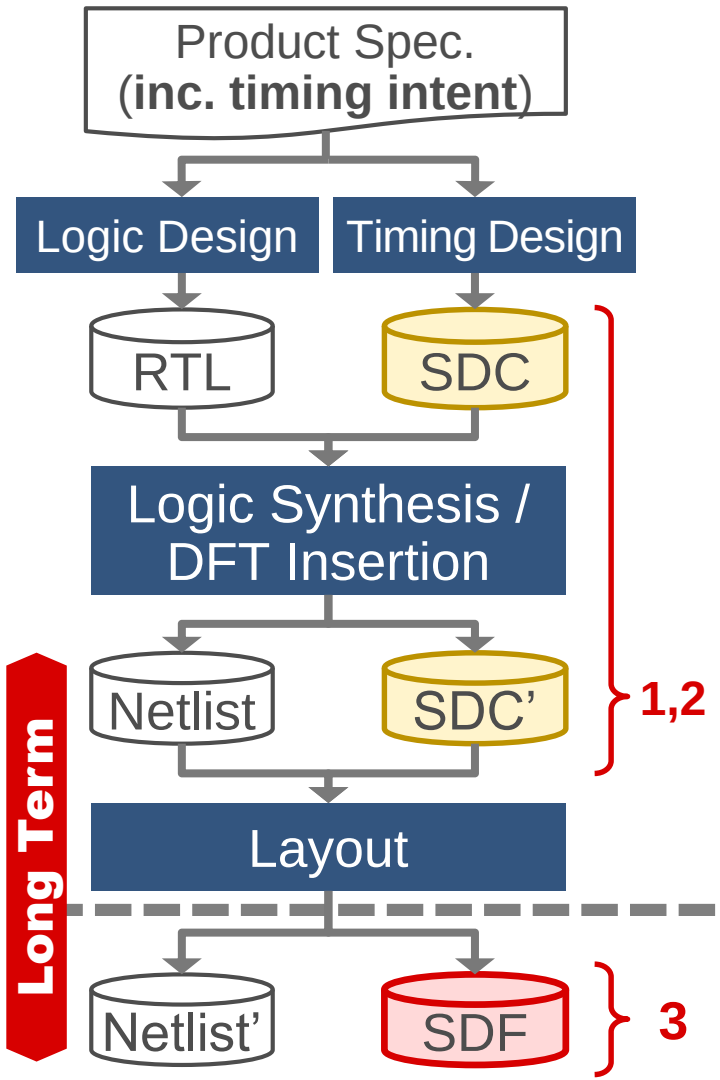
Agenda

- Current Design Flow and SDC Verification Method
- A Benefit of The Early Detection of SDC Issue : Shift Left
- The Concept of Our ABSV (Assertion Based SDC Verification)
- Examples of SVA Generation
  - Generated Clock and Multi-Cycle Path
- Application Results
- Summary

Current Design Flow and SDC Verification Method



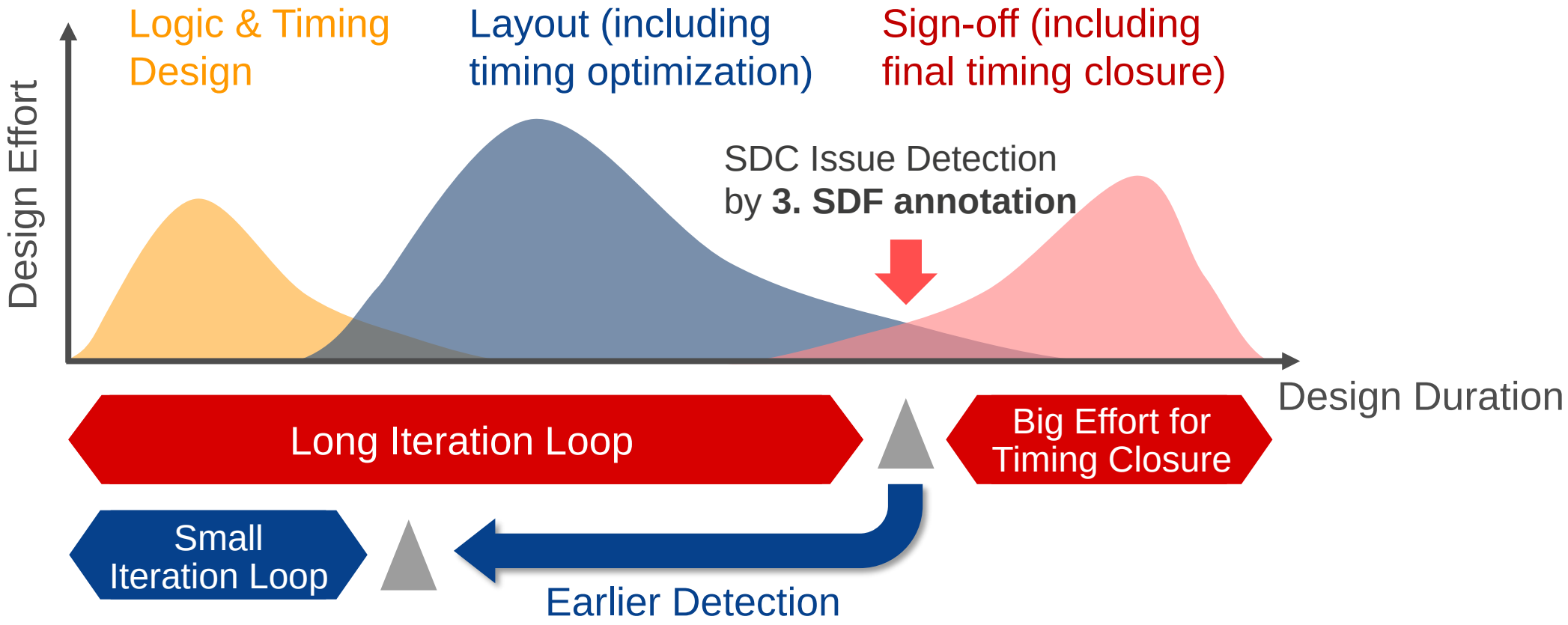
- The SDC (Timing Constraint) is as important as HDL (Hardware Description) for correct chip operation.
- The coverage of SDC verification by simulation with SDF (Delay) is good enough, however it is too late.

Traditional SDC Verification Methods

Methods	Explanation	Coverage	Applicable Phase
1. Rule-based Check	Static checking the SDC commands w/ predefined rule	Only syntax & semantics	Early
2. Formal Verification	Static checking the consistency b/w SDC and circuit structure	Limited (Small size & particular circuit)	Early
3. SDF Annotation	Simulation w/ SDF generated after layout	Better (Test bench dependent)	Very Late

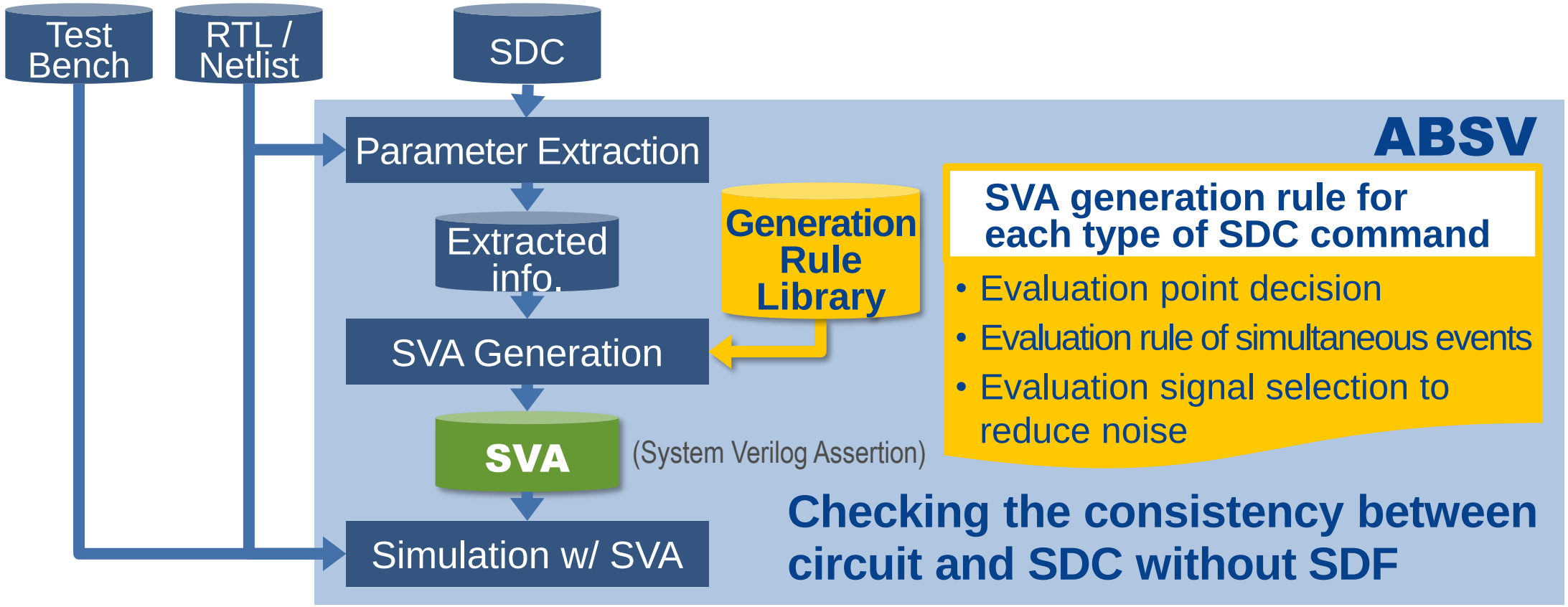
A Benefit of The Early Detection of SDC Issue : Shift Left

- The earlier detection of SDC issue can save more design effort and improve the productivity.



The Concept of Our ABSV (Assertion Based SDC Verification)

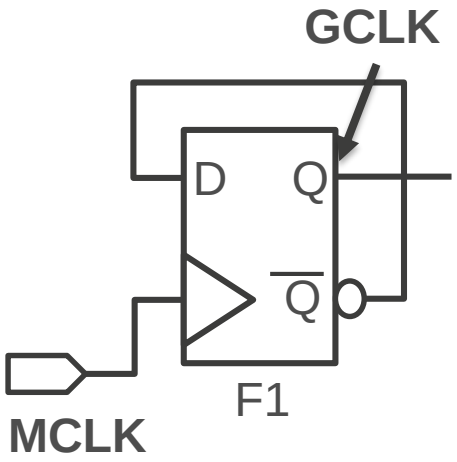
- Our solution is the generation of SVA defining the '**Circuit Behavior**' described in SDC, to enable SDC verification without SDF.



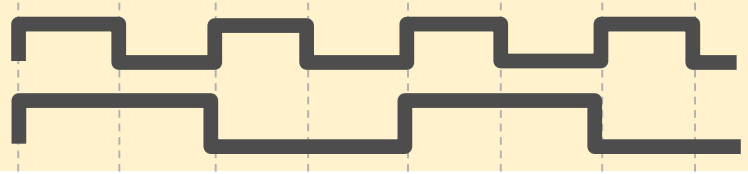
Example 1. SVA Generation for Generated Clock

- One example of the coverage improvement of ABSV is generated clock.

SDC	*create_clock -name MCLK -period 20 -waveform {0 10} [get_ports Port]* *create_generated_clock -name GCLK -divide_by **2** -source [get_ports Port] [get_pins F1/Q]*
Timing Intent	The generated clock GCLK changes on every two edges of master clock MCLK

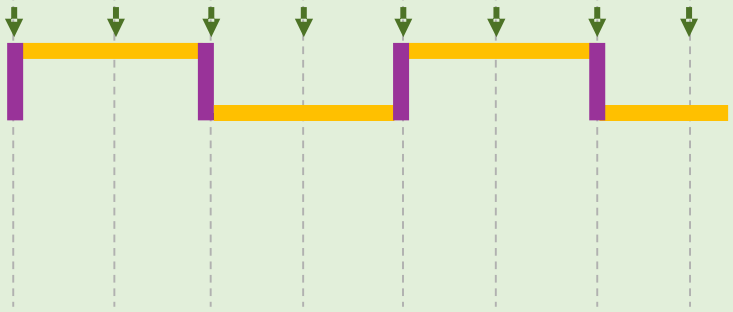


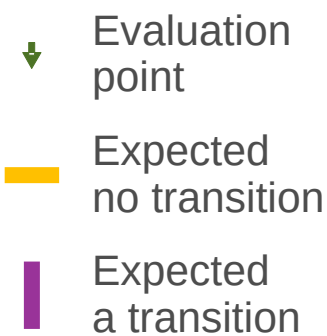
Simulation Results (Golden)



Generated SVA

From **correct SDC**

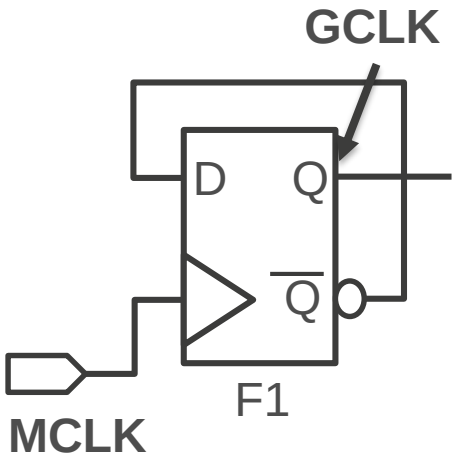




Example 1. SVA Generation for Generated Clock

- One example of the coverage improvement of ABSV is generated clock.

SDC	*create_clock -name MCLK -period 20 -waveform {0 10} [get_ports Port]* *create_generated_clock -name GCLK -divide_by **4** -source [get_ports Port] [get_pins F1/Q]*
Timing Intent	The generated clock GCLK changes on every **four edges** of master clock MCLK



Simulation Results (Golden)

Master Clock - MCLK

Generated clock - GCLK

Generated SVA

From **correct SDC**

From **wrong SDC**
e.g. **-divide_by 4**

Detect inconsistency

Evaluation point

Expected no transition

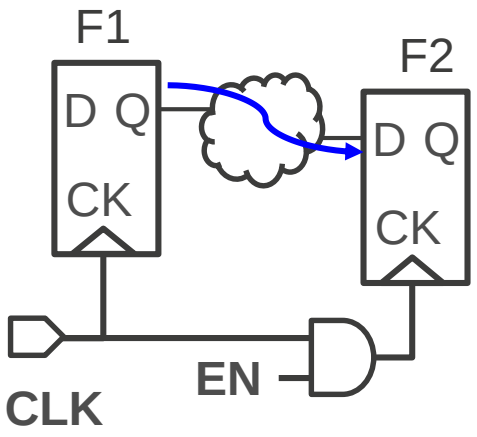
Expected a transition

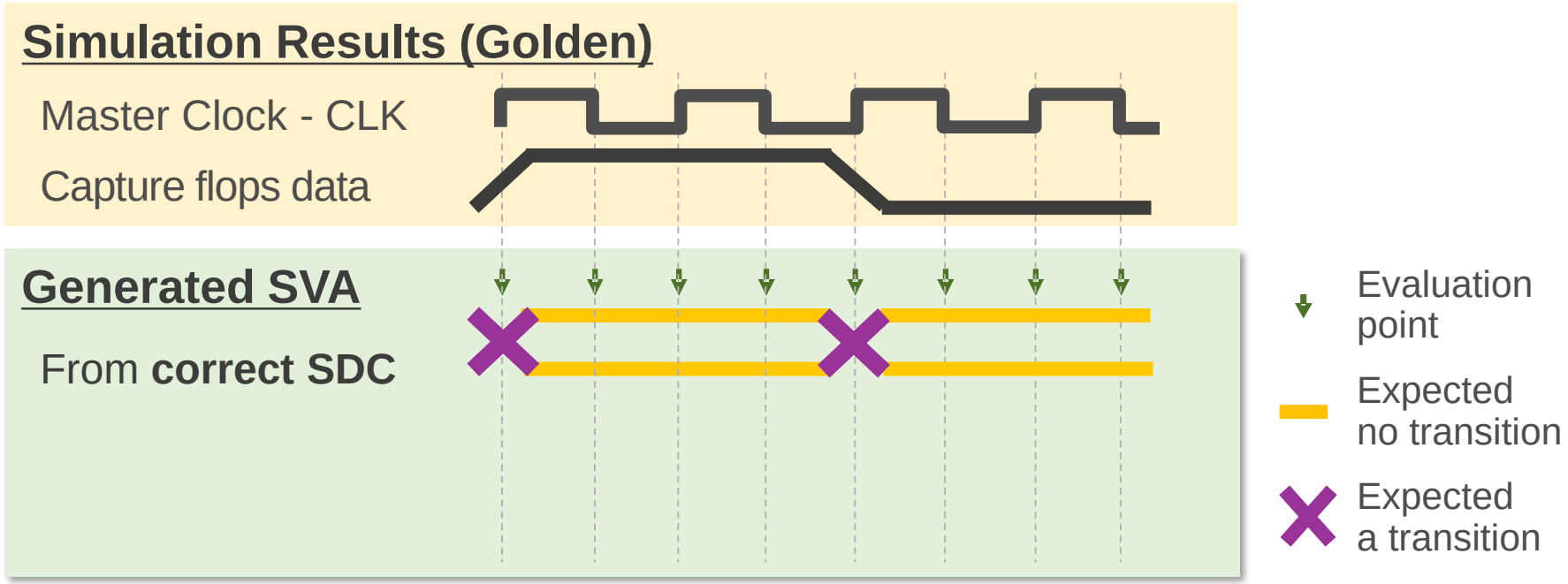
Example 2. SVA Generation for Expectations (MCP case)

- The coverage of SDC verification is expanded to timing exception by ABSV.

SDC	*set_multicycle_path 2 -from [get_clocks CLK] -through [get_pins F1/Q] -to [get_pins F2/D]*
Timing Intent	The value latched at the endpoint F2 does not change within the specified two cycles

Multi-Cycle Path
(2 cycle transfer)

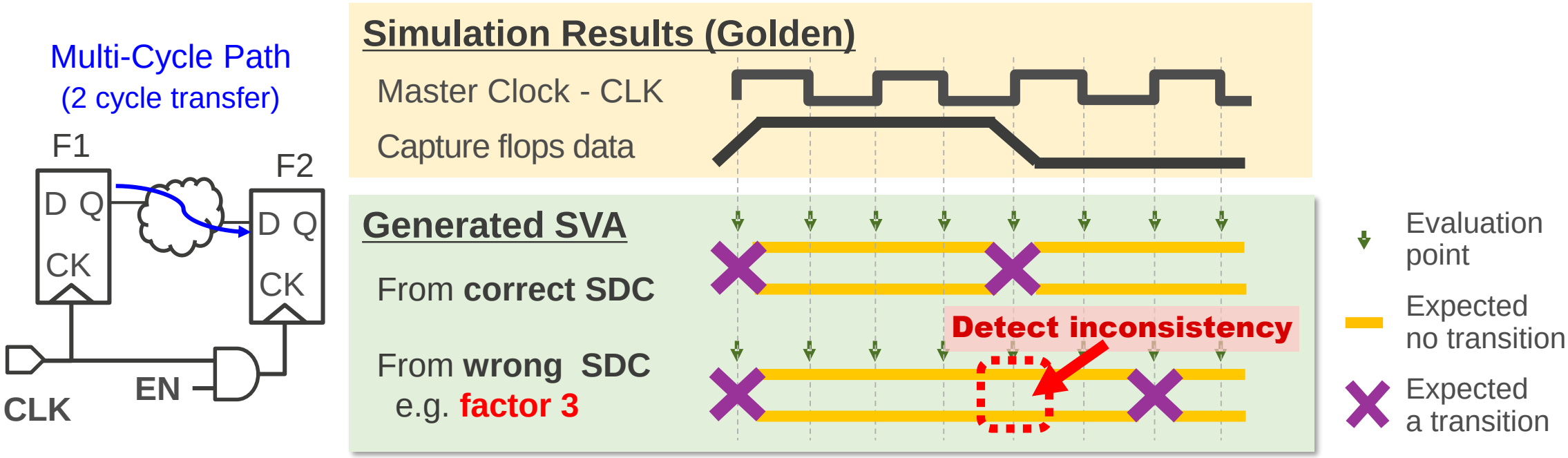




Example 2. SVA Generation for Expectations (MCP case)

- The coverage of SDC verification is expanded to timing exception by ABSV.

SDC	*set_multicycle_path **3** -from [get_clocks CLK] -through [get_pins F1/Q] -to [get_pins F2/D]*
Timing Intent	The value latched at the endpoint F2 does not change within the specified **three cycles**



Coverage Improvements by Our ABSV

- We've **expanded the coverage** of SDC verification **by ABSV** in addition to Rule-based check and Formal verification.

Coverage of Each Verification Method

Check Points	SDC Command	Rule-based Check	Formal Verification	ABSV
Syntax / Semantic	All	Available	-	-
Structure consistency	MCP & FP	N/A	Available	-
Timing Intent consistency	**Generated clock**	N/A	N/A	**Available**
	MCP & FP	N/A	N/A	**Available**

MCP : Multi Cycle Path, FP: False Path, N/A : Not Available

Application Results : Simulation with SVA is Quick Enough

- The number of generated SVA is quite large, however the verification time is quick enough.
- Since we can execute the ABSV and layout in parallel, there is no overhead of design duration.

The number of generated SVA and simulation execution time for SDC Verification

No	Design Information		Number of Generated SVA	Execution Time of SVA Generation & Simulation with SVA	Simulation with SDF Annotation (Traditional flow)
	# Instances	# SDC commands			
1	0.5 M	0.1 K	0.6 K	**5.1 Hours**	1 Week
2	20 M	30 K	1,947 K	**5.4 Days**	1 Month
3	40 M	600 K	18,039 K	**11.6 Days**	2 Months

Summary

- We’ve developed the method of “**ABSV** (Assertion based SDC verification)” to detect the SDC issues related to timing intent in early design phase.
- The method offers the following advantages ;
  - The coverage of **earlier phase SDC verification** is improved.
  - The coverage improvement **reduces the chance of big iteration loop** caused by immature SDC.
  - The automatic SVA generation with Excellicon’s tools **dismisses concern about human error**.

Thank you